Listing of Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

1. (Previously Presented) A memory module comprising:

a printed circuit board having a plurality of connector pins;

a plurality of different types of memory devices mounted on said printed circuit board; and

an electrical circuit coupling said plurality of memory devices to said plurality of connector pins such that said plurality of connector pins has multiple functionality based on a respective architecture of each of said plurality of different types of memory devices.

2. (Previously Presented) The memory module according to claim 1 wherein said different types of memory devices are selecting from the group consisting of Double Data Rate Synchronous Dynamic Random Access Memory (DDR SDRAM), a Fast Cycle Random Access Memory (FCRAM), and a Reduced Latency Dynamic Random Access Memory (RLDRAM).

3. (Original) The memory module according to claim 1 wherein said plurality of connector pins engages with a memory socket, said memory socket communicating with a memory controller.

4. (Previously Presented) The memory module according to claim 3 wherein said memory controller includes:

a plurality controllers, each controller corresponding to an architecture of one of the plurality of different types of memory devices;

a Finite State Machine (FSM) coupled to said plurality of controllers;

an address multiplexor coupled to said FSM, said address multiplexor communicating with said memory socket;

a control multiplexor coupled to said FSM, said control multiplexor communicating with said memory socket; and

a data multiplexor coupled to said FSM, said data multiplexor communicating with said memory socket.

5. (Previously Presented) The memory module according to claim 1 further comprising:

a second electrical circuit for testing said plurality of different types of memory devices, said second electrical circuit coupled to said plurality of different types of memory devices; and

a plurality of testing pins coupled to said second electrical circuit.

6. (Original) The memory module according to claim 5 wherein said second electrical circuit supports a JTAG configuration.

7. (Original) The memory module according to claim 1 wherein said plurality of connector pins includes 220 pins.

8. (Previously Presented) A computer comprising:

a main board; and

a memory module coupled to said main board, said memory module including:

a printed circuit board having a plurality of connector pins; and

a plurality of different types of memory devices mounted on said printed circuit board,

an electrical circuitry electrically coupling said plurality of memory devices to said plurality of connector pins such that said plurality of connector pins has multiple functionality based on an architecture of each memory device.

9. (Previously Presented) The computer of claim 8 wherein the architecture of the plurality of different types of memory devices is selected from the group consisting of a DDR SDRAM, a FCRAM, and a RLDRAM.

10. (Previously Presented) A method for mounting a plurality of different types of memory devices with different configurations on a single memory module having a plurality connector pins, said method comprising:

electrically coupling the plurality of different types of memory devices on the memory module, each memory device having different configurations;

connecting the memory devices to the plurality of connector pins; and

configuring the connection between the memory devices and the plurality of connector pins such that the connector pins have multiple functionalities based on an architecture of each of the memory devices.

11. (Previously Presented) The method of claim 10 wherein the architecture of the plurality of different types of memory devices is selected from the group consisting of a DDR SDRAM, a FCRAM, and a RLDRAM.